Preface

Recently, video coding has become pervasive due to the availability of devices able to act as video co-decoders. Stemming from the MPEG2 standard, several new algorithms and techniques have been proposed to improve the coding efficiency of modern video coding systems. These techniques include different parts of the compression/decompression chain, such as transform stages, entropy coding, motion estimation, intra prediction, and filtering. For these reasons, in the last twenty years, video compression started facing new challenges. High quality/high resolution sequences, virtual reality and immersive gaming have pushed video compression standards toward new directions. In 2013, the High Efficiency Video Coding (HEVC) standard, jointly developed by VCEG and MPEG in a Joint Collaborative Team on Video Coding (JCT-VC), has been published. HEVC is able to achieve twice better compression efficiency compared to the AVC standard. Namely, the same subjective video quality is achieved at twice lower bitrate compared to the High Profile of AVC. Thus, with the HEVC standard the computational complexity has become really impressive. Moreover, one of the key objectives of HEVC was to focus on high resolution video coding. All these aspects brought to new challenges from the implementation point of view, fostering researchers to find new approaches and paradigms to reach efficient memory handling, low power consumption and high parallelization. As a consequence, new highly optimized VLSI architectures were proposed in the literature showing that these results can be obtained by combining deep knowledge of implementation aspects with a good background in video coding fundamentals. One of the effects of this cross-layer approach has been to bring the approximate computing paradigm as a promising solution for future video coding VLSI architectures. Concurrently, the JCT-VC started working on the next video compression standard: Versatile Video Coding (VVC) which is expected to be finalized in 2020. Thus, opening a new scenario for hardware implementation.

This book tries to cover the main aspects related to the implementation of VLSI architectures tailored to future video coding. For this reason the book addresses several hardware-implementation-related topics, including scalable transform architectures, joint algorithm-architecture design, high throughput architectures and low power techniques for high resolution video coding, 3D video coding and frame memory compression. Moreover, the books includes also important examples and cases of study, by showing how the approximate computing paradigm can exploited to reduce the complexity of the transform stage and to design reconfigurable and multi-frequency architectures. Finally, the book provides some future perspectives by presenting new tools and algorithms, which are likely to be part of the forthcoming VVC standard.

Maurizio MARTINA